Electronic Devices and Circuits

EME306

(Summer 2021-2022)

Lecture 6

Bridge Rectifier, Filters and Regulators

INSTRUCTOR

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1) The bridge rectifier uses four diodes.
2) Peak Inverse Voltage
3) Power Supply , Filters and Regulators
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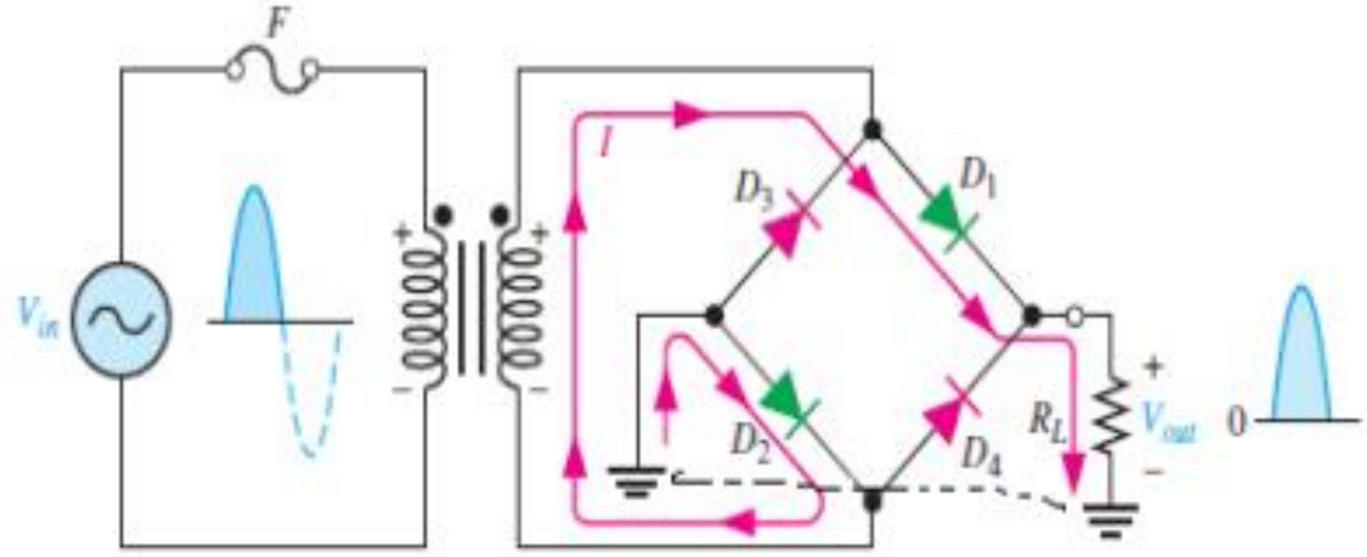
The bridge rectifier uses four diodes.

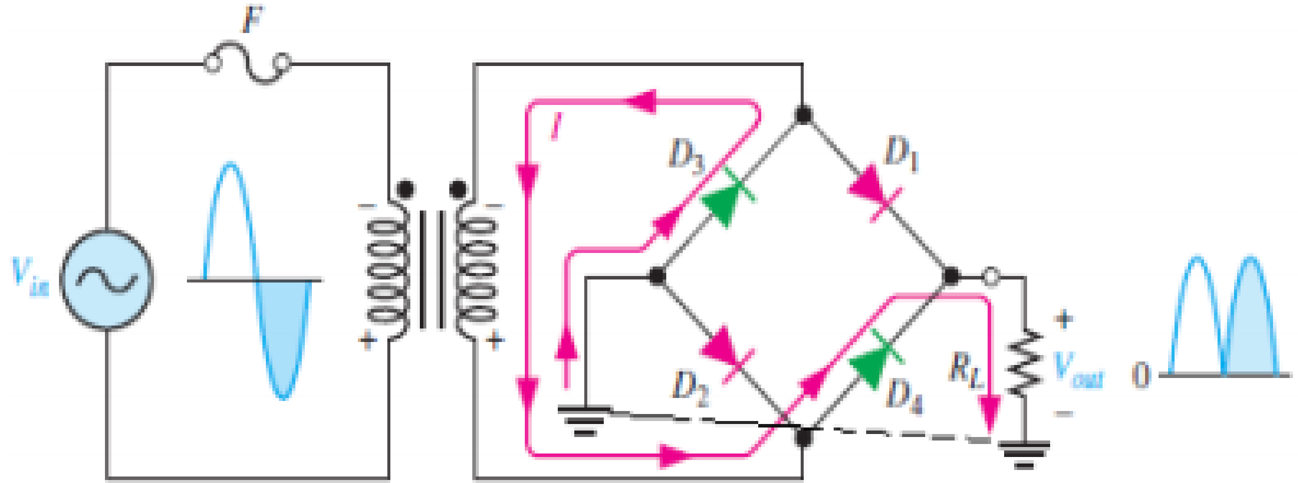
- For +ve half Cycle Diodes D1 and D2 are forward-biased and conduct current in the direction shown. While D3, D4 are reverse biased and off



- A voltage is developed across RL that looks like the positive half of the input cycle

For -ve half Cycle

- Diodes D3 and D4 are forward-biased and conduct current in the direction shown. While D1, D2 are reverse biased and off

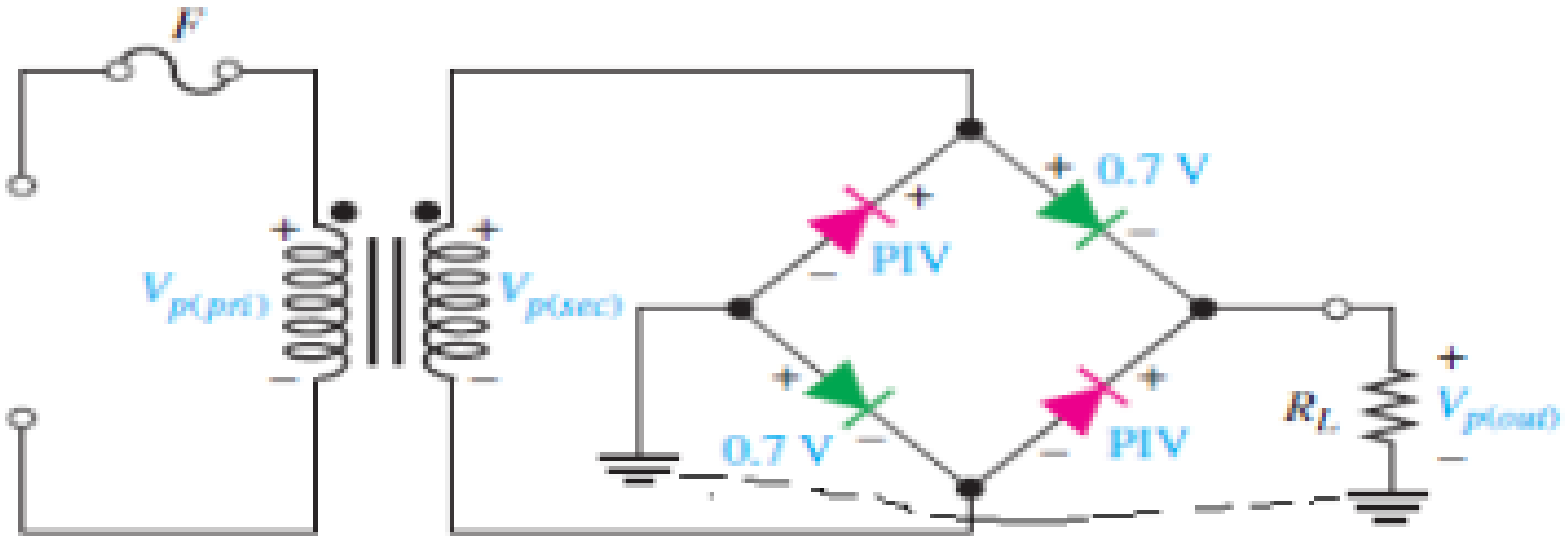


- A voltage is developed across RL that looks like the positive half of the input cycle

$$Vp_{(out)} = Vp_{(sec)} - 2*(0.7) = Vp_{(sec)} - 1.4\ V$$

Peak Inverse Voltage

- Let's assume that D1 and D2 are forward-biased and examine the reverse voltage across D3 and D4.



$$PIV = V_{p(out)} + 0.7 = V_{p(sec)} - 1.4 + 0.7$$

$$PIV = V_{p(sec)} - 0.7$$

Comparison

	Center taped Rectifier	Bridge Rectifier
Number of diodes	2	4
Vp(out)	$(V_{PSec}/2)-0.7$	$V_{PSec}-1.4$
PIV	$2V_{p(out)} + 0.7\ V$	$V_{p(out)} +0.7\ V$

Example

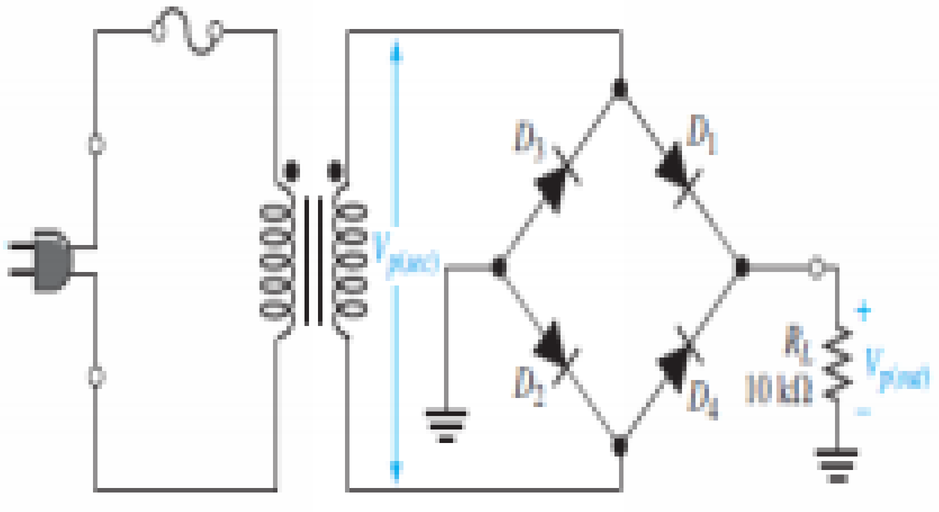
- The transformer is specified to have a 12 V rms secondary voltage for the standard 120 V across the primary.
  - (a) Determine the peak output voltage for the bridge rectifier in Figure.
  - (b) Assuming VD=0.7 when on, what PIV for the diodes?.

Given $V_{sec(rms)}=12v$

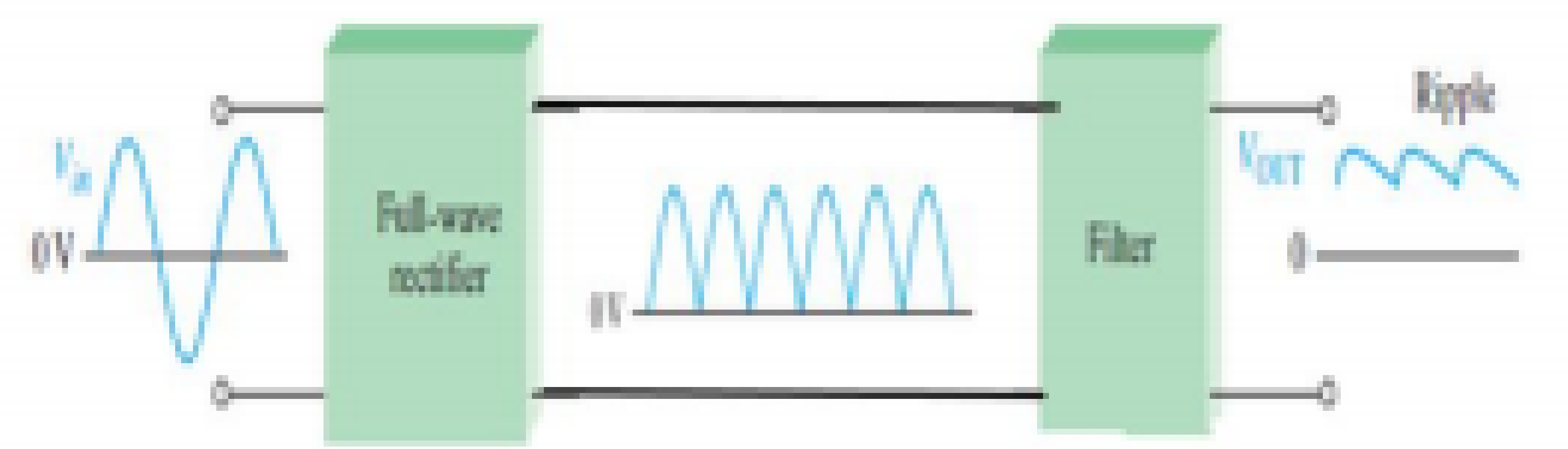
$$V_{Peak(sec)} = V_{P(sec)} = \sqrt{2}V_{sec(rms)} = 1.414*12 = 16.971v$$

$$V_{P(out)} = V_{P(sec)} - 1.4 = 16.971 - 1.4 = 15.571v$$

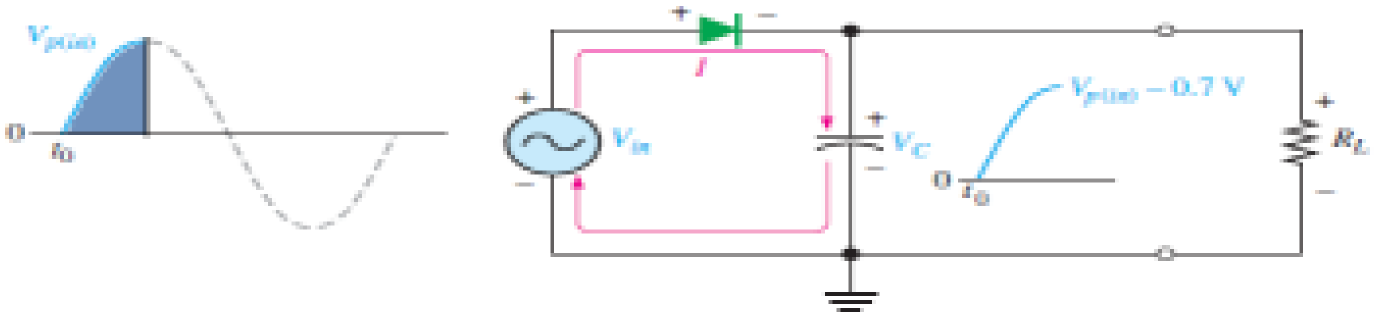
$$PIV = V_{P(out)} + 0.7 = 15.571 + 0.7 = 16.271v$$



Power Supply , Filters and Regulators

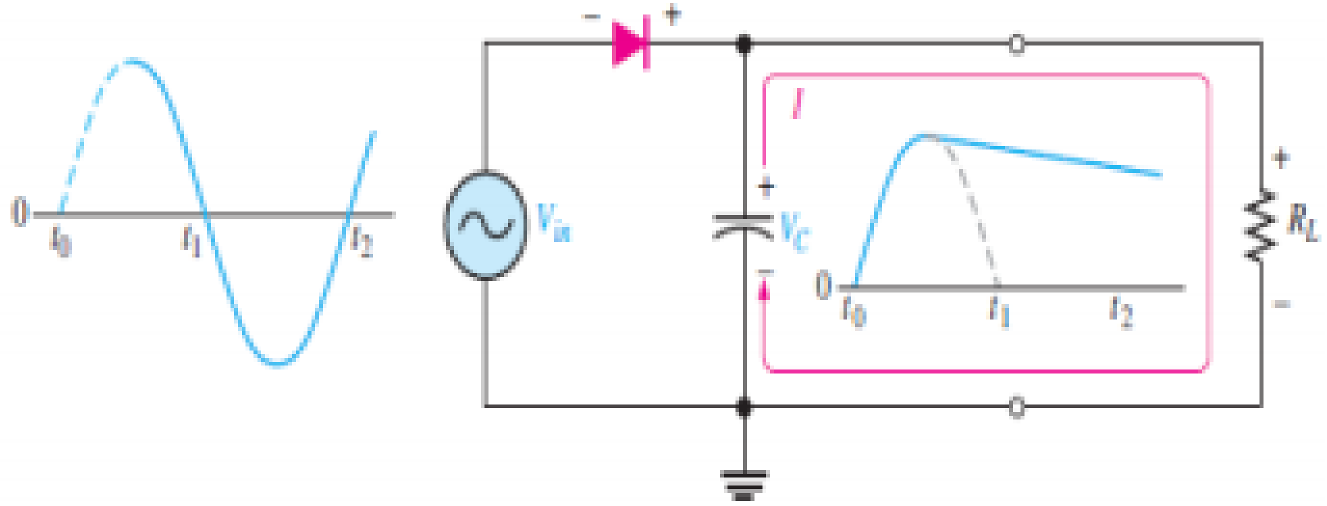


- Capacitor-Input Filter During the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to Vp(in)-0.7



Power Supply , Filters and Regulators

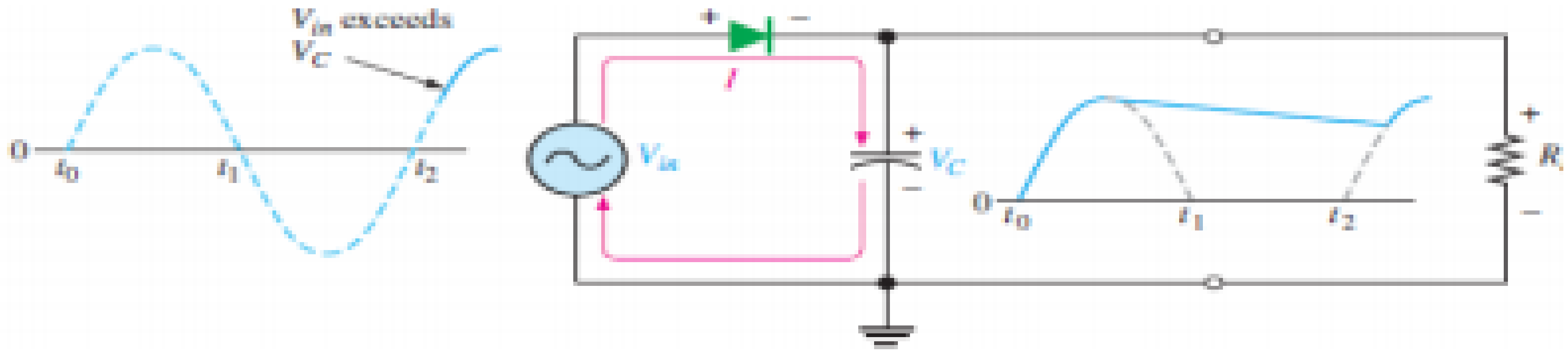
- When the input begins to decrease below its peak (in the 2nd quarter)
  - The diode becomes reverse-biased.
  - So , the capacitor can discharge only through the load with time constant t= RC which is normally long compared to the period of the input.



- The larger the time constant, the less the capacitor will discharge.

Power Supply , Filters and Regulators

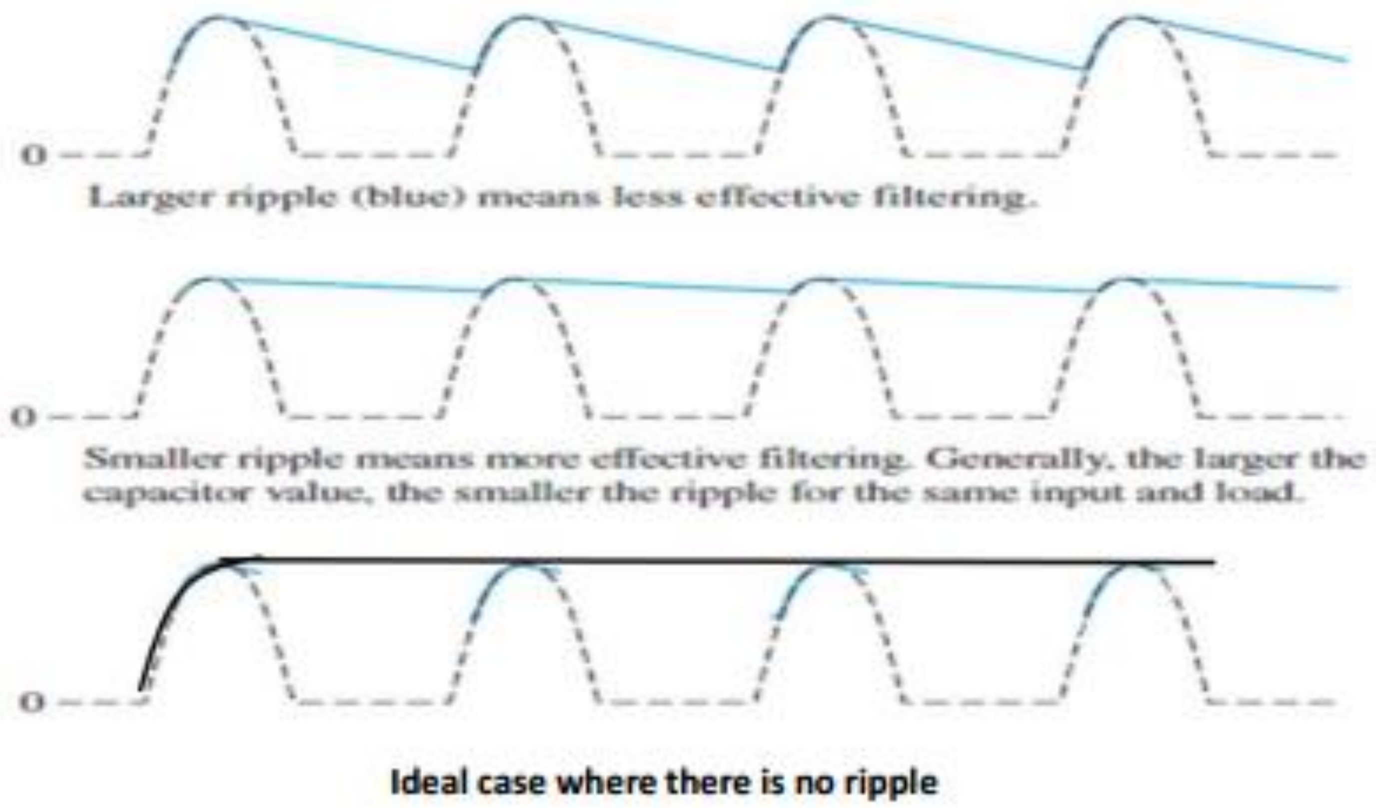
- During the first quarter of the next cycle, the diode will again become forward-biased when the input voltage exceeds the capacitor voltage by approximately 0.7 V.



- Ripple Voltage
  - The capacitor quickly charges at the beginning of a cycle.
  - slowly discharges through RL after the positive peak of the input voltage (when the diode is reverse-biased).
  - The variation in the capacitor voltage due to the charging and discharging is called the ripple voltage

Power Supply , Filters and Regulators

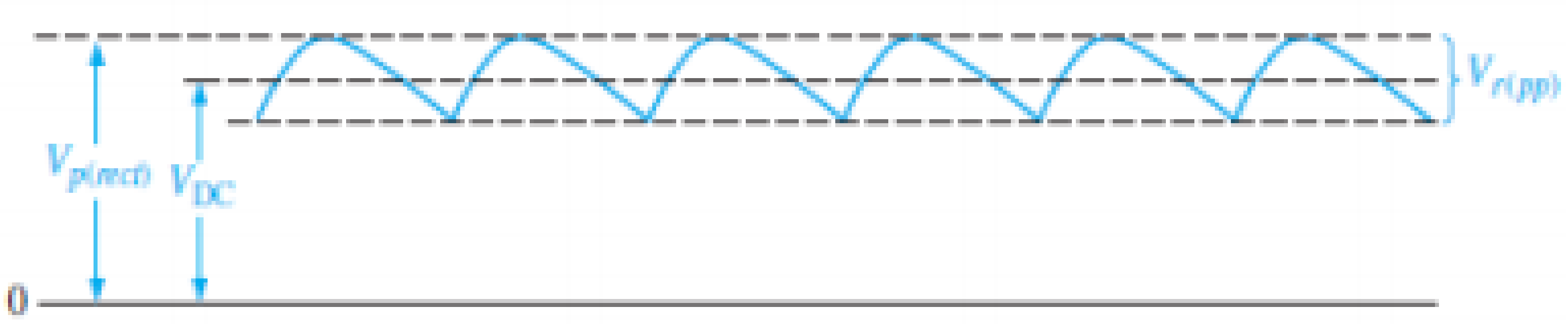
- Generally, ripple is undesirable; thus, the smaller the ripple, the better the filtering action, as illustrated in



Ripple Factor

- The ripple factor (r) is an indication of the effectiveness of the filter and is defined as

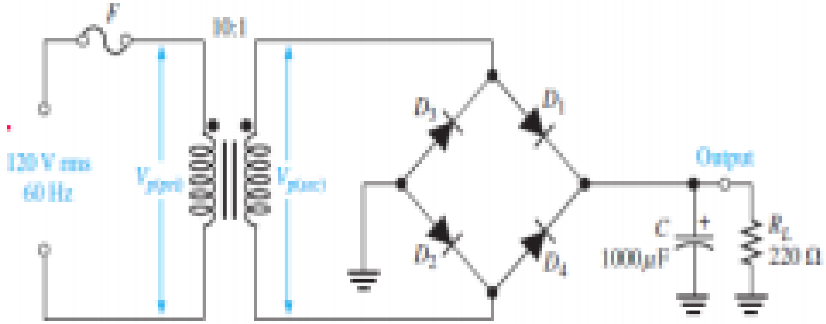
$$r = \frac{V_{r(pp)}}{V_{DC}}$$



- The lower the ripple factor, the better the filter.
- The ripple factor can be lowered by increasing capacitor value of or the load resistance.

EXAMPLE

- Determine the ripple factor for the filtered bridge rectifier as indicated.



$V_{p(pri)} = 1.414V_{rms} = 1.414(120\text{ V}) = 170\text{ V}$

$V_{p(sec)} = nV_{p(pri)} = 0.1(170\text{ V}) = 17.0\text{ V}$

The unfiltered peak full-wave rectified voltage is

$V_{p(rect)} = V_{p(sec)} - 1.4\text{ V} = 17.0\text{ V} - 1.4\text{ V} = 15.6\text{ V}$

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{P(rect)} = \left(\frac{1}{120Hz*220\Omega*1000\mu F}\right)*15.6 = 0.591V$$

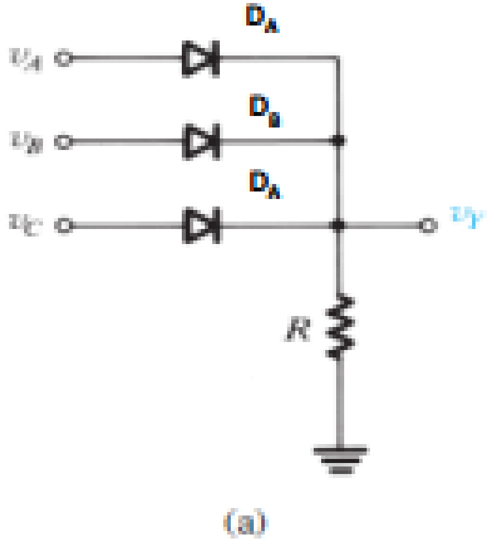
$$V_{DC} = \left(V_{P(rect)} - \frac{V_{r(pp)}}{2}\right) = \left(1 - \frac{1}{2fR_LC}\right)V_{P(rect)} = \left(1 - \frac{1}{2*120Hz*220\Omega*1000\mu F}\right)*15.6 = 15.3V$$

$$r = \frac{V_{r(pp)}}{V_{DC}} = \frac{0.591}{15.3} = 0.039$$

Another Application: Diode Logic Gates

- OR gate

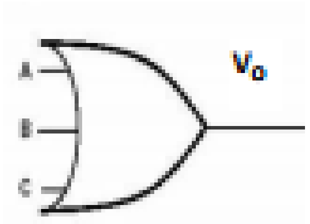
V_A	V_B	V_C	D_A	D_B	D_C	V_o		V_A	V_B	V_C	V_o
0v	0v	0v	off	off	off	0v		0	0	0	0
0v	0v	5v	off	off	on	5v		0	0	1	1
0v	5v	0v	off	on	off	5v		0	1	0	1
0v	5v	5v	off	on	on	5v		0	1	1	1
5v	0v	0v	on	off	off	5v		1	0	0	1
5v	0v	5v	on	off	on	5v		1	0	1	1
5v	5v	0v	on	on	off	5v		1	1	0	1
5v	5v	5v	on	on	on	5v		1	1	1	1



(a)

It represent an **OR logic gate**

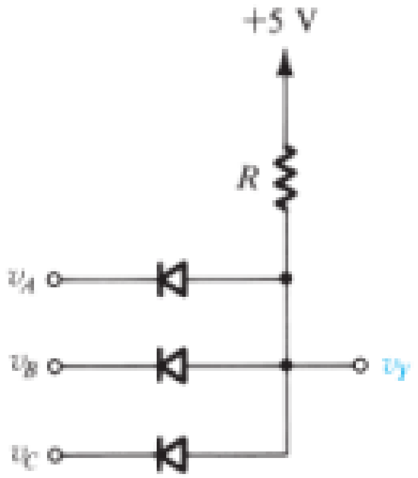
$V_o = V_A + V_B + V_C$



Another Application: Diode Logic Gates

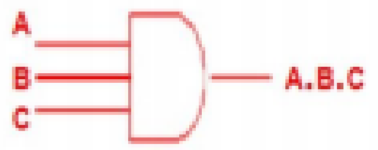
- And gate

V_A	V_B	V_C	D_A	D_B	D_C	V_o		V_A	V_B	V_C	V_o
0v	0v	0v	on	on	on	0v		0	0	0	0
0v	0v	5v	on	on	off	0v		0	0	1	0
0v	5v	0v	on	off	on	0v		0	1	0	0
0v	5v	5v	on	off	off	0v		0	1	1	0
5v	0v	0v	off	on	on	0v		1	0	0	0
5v	0v	5v	off	on	off	0v		1	0	1	0
5v	5v	0v	off	off	on	0v		1	1	0	0
5v	5v	5v	off	off	off	5v		1	1	1	1



It represent an AND logic gate

$V_o = V_A . V_B . V_C$




Thank you